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JC885 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)*(Only for new nonprovisional applications under 37 CFR 1.53(b))*Docket No.
11675.76.3Total Pages in this Submission
18

JC784 U.S. PTO

07/28/00

TO THE ASSISTANT COMMISSIONER FOR PATENTSBox Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

INTERLEVEL DIELECTRIC STRUCTURE

and invented by:

Gurtej S. Sandhu, Anand Srinivasan and Ravi IyerIf a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 08/677,514

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 18 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☒ Cross References to Related Applications *(if applicable)*
 - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
 - d. ☐ Reference to Microfiche Appendix *(if applicable)*
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings *(if drawings filed)*
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
- a. ☒ Formal Number of Sheets 5
- b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
- a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
- b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
- c. ☐ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under
Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy *(identical to computer copy)*
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
- ☐ First Class ☒ Express Mail *(Specify Label No.):* EL 569 075 038 US

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

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Docket No.
11675.76.3

Total Pages in this Submission
18

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. ☐ Additional Enclosures (please identify below):

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	12	- 20 =	0	x \$18.00	\$0.00
Indep. Claims	1	- 3 =	0	x \$78.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$690.00

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Signature

Bradley K. DeSandro, Reg. No. 34,521

Dated: July *27*, 2000



22901

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(General - Patent Pending)**

Docket No.
11675.76.3

In Re Application Of: Sandhu et al.

Serial No.
Not yet assigned

Filing Date
Herewith

Examiner
Not yet assigned

Group Art Unit
Not yet assigned

jc734 U.S. PTO
09/627649



Title: INTERLEVEL DIELECTRIC STRUCTURE

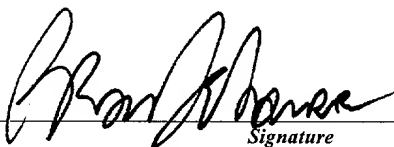
TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Utility Patent Application Transmittal Letter (3 pgs); Divional Patent Application (18 pgs); Declaration and Oath; Assignment; Five (5) Sheets of Formal Drawings; Form PTO-2038; Certificate of Mailing by Express Mail, No. EL 569 075 038 US; Postcard

in the above identified application.

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Dated: July 27, 2000

Bradley K. DeSandro, Reg. No. 34,521



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Serial No. Not yet assigned	Filing Date Herewith	Examiner Not yet assigned		Group Art Unit Not yet assigned
Invention: INTERLEVEL DIELECTRIC STRUCTURE				


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 37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on
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Express Mailing Label No. EL 569 075 038 US

Docket No. 11675.76.3

UNITED STATES PATENT APPLICATION

of

GURTEJ S. SANDHU

ANAND SRINIVASAN

and

RAVI IYER

for

INTERLEVEL DIELECTRIC STRUCTURE

003749 2390

BACKGROUND OF THE INVENTION

This application is a divisional application of United States Patent Application Serial No. 677,514, filed on July 10, 1996, which is incorporated herein by reference.

1. The Field of the Invention

The present invention relates to the design and manufacture of interlevel dielectrics in the manufacture of semiconductor devices. More particularly, the present invention relates to the design and manufacture of interlevel dielectrics in the manufacture of semiconductor devices in which the dielectric constant of the interlevel dielectric is less than about 3.6.

2. The Relevant Technology

The continuing trend in the semiconductor industry of squeezing more and more circuit devices into a given area has resulted in significant improvements in the performance of individual integrated circuits and of electronic devices that employ integrated circuits. In a typical integrated circuit, individual circuit elements or groups of elements are generally electrically connected together by a metallization process, in which layers of metal are deposited and patterned to form metal lines which complete the circuit as designed. Multiple metal layers are often employed. Metal lines within patterned metal layers are insulated by layers known as interlevel dielectrics. The interlevel dielectrics insulate the metal lines from any undesired electrical contact both with other metal lines, whether in the same or another metal layer, and with other circuit elements.

The capacitance between two conductive materials is also affected by the material as well as the distance between them. The ratio of the capacitance between two conductors with a given material between them to the capacitance of the same two conductors with nothing (a vacuum) between them is known as the dielectric constant of the given material. Thus a material with a high dielectric constant placed between two conductors increases the capacitance between the two conductors.

One way to gain some of the benefits of low dielectric constant materials is shown in Figure 1. Figure 1 is a partial cross section of a partially formed integrated circuit device. A substrate or lower layer 12 has a first dielectric layer 14 comprised of a traditional dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal, overlie first dielectric layer 14. A material with a dielectric constant lower than that of silicon dioxide 18 is located in between lines of conductive material 16. Lines of conductive material 16 together with low dielectric constant dielectric material 18 are covered by a second dielectric layer 21 comprised of a traditional dielectric material such as silicon dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low dielectric constant dielectric material 18 from other portions of the integrate circuit. Second dielectric layer 21 allows further processing, including formation of contact holes for contacting lines of conductive material 16 such as contact hole 46, without exposing dielectric material 18 to processing agents.

1 polished back to the additional layer. The additional layer is then optionally removed before
2 a second dielectric layer is deposited over all.

3 Yet another preferred method for forming the interlevel dielectric structure includes
4 providing a metal layer on a first dielectric layer, then patterning the metal layer with an over
5 etch into but not through the first dielectric layer to form metal lines with spaces
6 therebetween. A thin layer of silicon dioxide is then deposited by a method providing
7 preferential deposition on the upper surfaces of the metal lines. The thin layer of silicon
8 dioxide is then optionally etched, and a dielectric material is then deposited to fill the spaces
9 and is then etched or chemically mechanically polished back. A second dielectric layer is
10 then deposited over all.

11 The above briefly described methods allow reliable formation of a desired interlevel
12 dielectric structure, which structure provides reduced total capacitance between adjacent
13 conductive lines needed for further miniaturization of integrated circuits.

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1 material 16 adjacent thereto, and a lower surface 30 lower than the lower surfaces 24 of lines
2 of conductive material 16 adjacent thereto.

3 The extension of dielectric material 17 below and above lines of conductive material
4 16 significantly reduces capacitance between adjacent pairs of lines of conductive material
5 16.

6 The electric field formed by a potential difference applied across an adjacent pair of
7 lines of conductive material 16 is strongest in a direct line and centrally between the adjacent
8 pair, such as along dashed line N in Figure 2. But the electric field so formed also extends
9 to a fringe area not in a direct line between the adjacent pair, such as along dashed line F in
10 Figure 2. The field in this area, called the fringe, is associated with a portion of the total
11 capacitance, the portion called herein "fringe capacitance," between the adjacent pair.

12 The portion of the total capacitance included in fringe capacitance increases as
13 aspect ratio (height/width) of lines of conductive material 16 decreases, and can be a
14 significant fraction of total capacitance at low aspect ratios. The extension of dielectric
15 material 17 below and above lines of conductive material 16 provides a low dielectric
16 material in the fringe areas of the electric field, thus reducing fringe capacitance and total
17 capacitance accordingly.

18 While dielectric material 17 extends below and above lines of conductive material
19 16, it does not extend directly over surface 26 or under surface 24. This allows formation
20 of contact holes such as contact hole 48 without exposing dielectric material 17 to processing
21 agents that could degrade dielectric material 17 or upper surface 26 at contact hole 48.

22 The above structure and variations thereon may be formed in a variety of ways,
23 presently preferred examples of which will be described below.

24 One preferred method of forming a structure of the present invention includes
25 providing a first dielectric layer 14 over the surface of a substrate of an underling layer 12,
26

1 then forming a conductive layer 34 and an additional layer 36 thereover, as shown in
2 Figure 3. Conductive layer 34 and additional layer 36 are then patterned by forming and
3 patterning a mask layer over additional layer 36, and then etching additional layer 36,
4 conductive layer 34, and a portion of first dielectric layer 14 at areas that are left exposed
5 through the mask layer. This results in spaces between adjacent remaining portions of
6 conductive layer 34.

7 Dielectric material 17 is then deposited to fill these spaces, and then removed from
8 the top downward to at least the top of the remaining portions of additional layer 36 by an
9 etch back or by chemical mechanical polishing. A second dielectric layer 21 is then
10 deposited over the substrate, resulting in the structure shown in Figure 4.

11 In Figure 4, lines of conductive material 16 are formed of the remaining portions of
12 conductive layer 34. Dielectric material 17 is deposited between lines of conductive material
13 16. If additional layer 36 is comprised of a suitable dielectric such as silicon dioxide, the
14 remaining portions of additional layer 36 may be incorporated into the inventive structure
15 as shown. Thus the remaining portion of additional layer 36 in Figure 4, together with
16 second dielectric layer 21, correspond to the depiction seen in Figure 2 as second dielectric
17 layer 20.

18 If additional layer 36 is not a dielectric, such as if titanium is used, for example, then
19 the remaining portions of layer 36 shown in Figure 4 are removed by an appropriate process
20 immediately before the deposition of second dielectric layer 20. This alternative additional
21 process step results in a structure like that which is shown in Figure 2.

22 Another preferred method of forming a structure of the present invention includes
23 providing a first dielectric layer over a substrate or an underlying layer, then depositing and
24 patterning a conductive layer over the first dielectric layer. During patterning of the
25 conductive layer, the conductive layer is over etched such that the first dielectric layer is
26

1 etched partially with the same pattern. Next, an additional layer is deposited over the
2 patterned metal layer by a deposition method having poor step coverage.

3 The results of the above steps are shown in Figure 5. First dielectric layer 14 has
4 been formed on substrate or underlying layer 12, and a conductive layer has been deposited
5 and patterned, leaving lines of conductive material 16. Additional layer 38 has been
6 deposited by a deposition method having poor step coverage. This results in additional layer
7 38 being formed substantially only on the upper surfaces of lines of conductive material 16
8 as shown.

9 If additional layer 38 is comprised of a suitable dielectric material, the further
10 process steps may proceed as before, with deposition and partial top-down removal of
11 dielectric material 17 and deposition of second dielectric layer 21, resulting in the structure
12 shown in Figure 7. The remaining portions of additional layer 38 are incorporated into the
13 inventive structure as shown, so that the remaining portion of additional layer 38 in Figure
14 5 together with second dielectric layer 21 in Figure 7, correspond to the depiction seen in
15 Figure 2 as second dielectric layer 20.

16 Silicon dioxide is the currently preferred material for additional layer 38, with
17 deposition by a silane and oxygen plasma enhanced chemical vapor deposition (PECVD)
18 being the preferred poor step coverage deposition method.

19 Figure 6 illustrates an optional etch step that may be included immediately after
20 deposition of additional layer 38 to remove lateral buildup of additional layer 38. The
21 preferred etch is a facet etch, and is preferably performed in an argon or an argon-plus-
22 fluorine based plasma. In a facet etch, additional layer 38 is etched slower at a top surface
23 thereof than it is etched at a corner thereof which connects the top surface to a lateral surface
24 thereof. The facet etch has the effect of removing substantially all of the lateral buildup
25 portions of additional layer 38 and the removed portions redeposit in semi-triangular form
26

at the base of the lines of conductive material 16 and first dielectric layer 14 interface. A continuous but thin lateral layer of additional layer 38 also deposits down the sides of lines of conductive material 16. Further processing as above then results in a structure like that which is shown in Figure 4, with the remaining portions of layer of additional material 36 corresponding to the remaining portions of additional layer 38. The redeposited fraction of additional material 38, however, remains thinly on the sides of lines of conductive material 16 and first dielectric layer 14.

If additional layer 38 is not a dielectric, or is otherwise not suitable to remain in place in the inventive structure, then additional layer 38 is removed by an appropriate process immediately before the deposition of second dielectric layer 21. This alternative additional process step results in a structure that is like that shown in Figure 2.

In yet another presently preferred method for forming a structure of the present invention, a first dielectric layer is provided over a substrate or an underlying layer, then a metal layer is deposited and patterned to form metal lines over the first dielectric layer. During patterning of the metal layer, the metal layer is over etched such that the first dielectric layer is etched partially with the same pattern. A thin silicon dioxide layer is then deposited conformably over the metal lines by a deposition process that deposits preferentially on the upper surface of the metal lines.

The above process results generally in the structure shown in Figure 8. First dielectric layer 14 is formed on substrate 12. Metal lines in the preferred form of aluminum lines 40 have been formed on first dielectric layer 14, and first dielectric layer 14 has been over etched in the same pattern as aluminum lines 40. A titanium nitride film 42 from a photolithography process used to pattern aluminum lines 40 remains on the upper surface of aluminum lines 40. While not required, inclusion of titanium nitride film 42 is presently preferred.

The preferred deposition process for selectively depositing a thin silicon dioxide layer 44 is an ozone based TEOS process, which preferentially deposits on TiN over silicon dioxide. Preferably, silicon dioxide layer 44 will be deposited only on titanium nitride film 42 and not on the sidewall of aluminum lines 40 as shown in Figure 8.

After deposition of silicon dioxide layer 44, the process may continue as with the other above processes by deposition and partial removal of a dielectric material 17, followed by deposition of second dielectric layer 21, resulting in the structure shown in Figure 9. Silicon dioxide layer 44 is incorporated into the inventive structure as shown, so that silicon dioxide layer 44 together with second dielectric layer 21 correspond to the depiction seen in Figure 2 as second dielectric layer 20.

As an alternative process step, an etch such as a facet etch in an argon or an argon-plus-fluorine based plasma may be performed on silicon dioxide layer 44 after the deposition thereof.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims and their combination in whole or in part rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured by United States Letters Patent is:

a dielectric material situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines.

3. The interlevel dielectric structure as defined in Claim 1, wherein at least one of the first and second dielectric layers comprises silicon dioxide.

1 4. The interlevel dielectric structure as defined in Claim 1, wherein said
2 conductive material is selected from the group consisting of polysilicon, aluminum, copper,
3 tungsten, and multiple layers of TiN/Al/TiN, TiN/Al/Ti, W/TiN/Ti, or any combinations
4 thereof.

6 5. The interlevel dielectric structure as defined in Claim 1, where the dielectric
7 material has a dielectric constant of less than about 3.6.

13. The interlevel dielectric structure as defined in Claim 6, where the dielectric material has a dielectric constant of less than about 3.6.

14. An interlevel dielectric structure comprising:

- a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;
- a plurality of lines comprised of a conductive material extending along said upper surface of said first dielectric layer; wherein:
 - each line of said plurality of lines has both a upper surface and a lower surface;
 - adjacent lines of said plurality of lines have spaces situated therebetween;
 - the lower surfaces of each line of said plurality of lines is in contact with said upper surface of said first dielectric layer;
 - the upper surface of at least one line of said plurality of lines has thereon a layer of titanium nitride;
 - said layer of titanium nitride has thereon a silicon dioxide layer; and
 - said silicon dioxide layer has thereon said second dielectric layer;
- a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the upper surface of each line of said plurality of lines; and
- a dielectric material situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, the upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, the lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines.

18. The interlevel dielectric structure as defined in Claim 14, where the dielectric material has a dielectric constant of less than about 3.6.

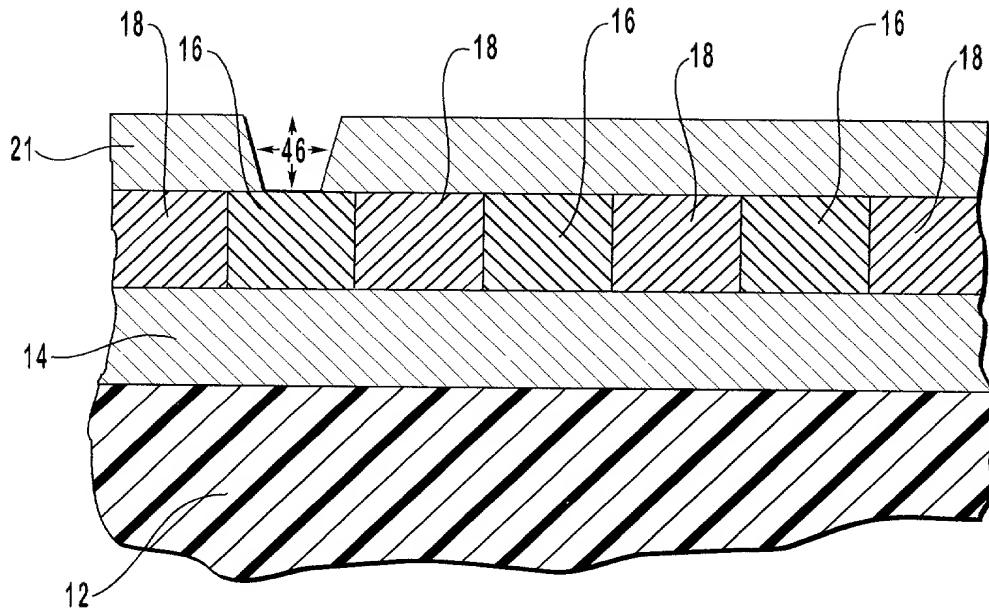


FIG. 1
(PRIOR ART)

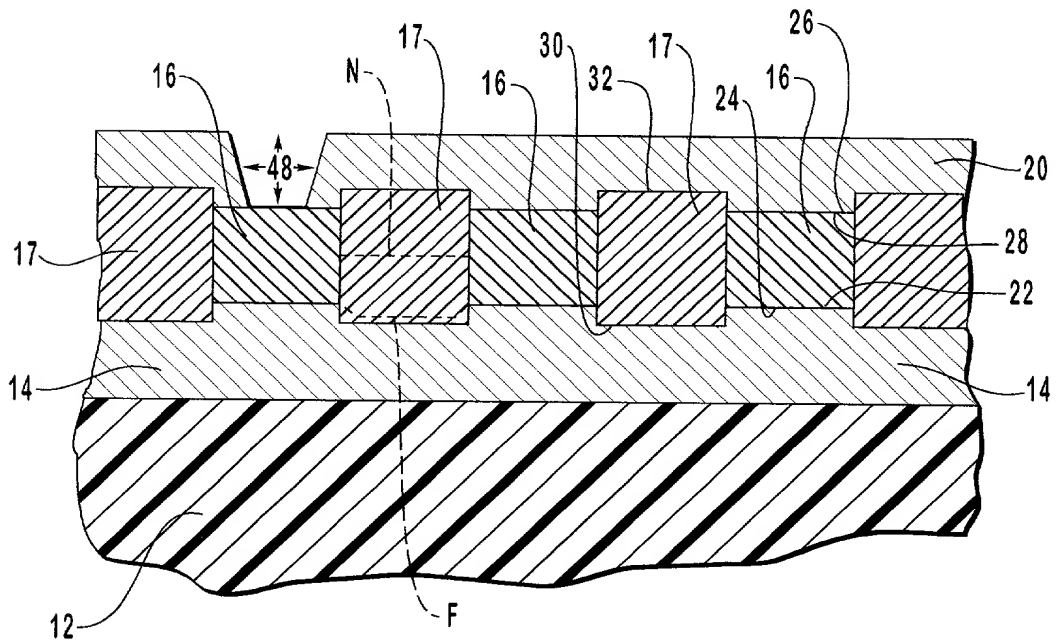


FIG. 2

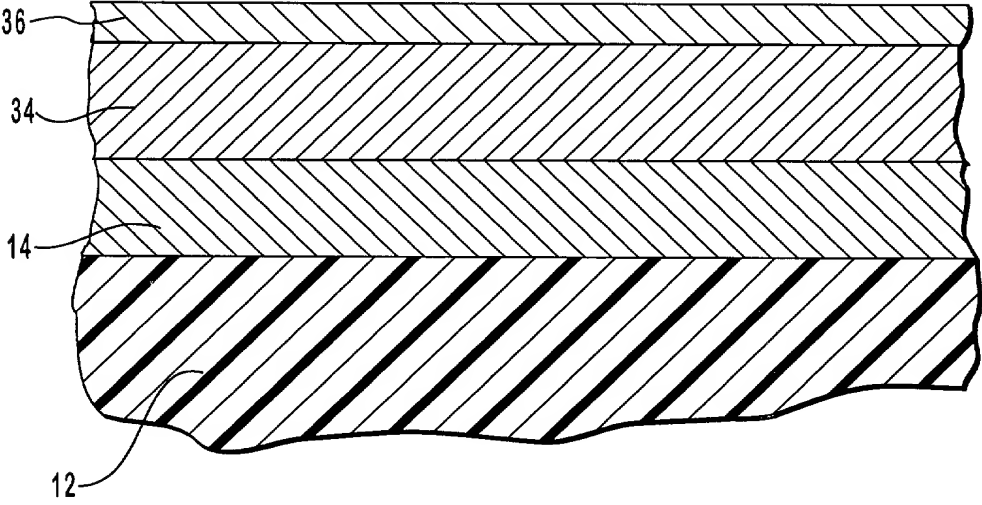


FIG. 3

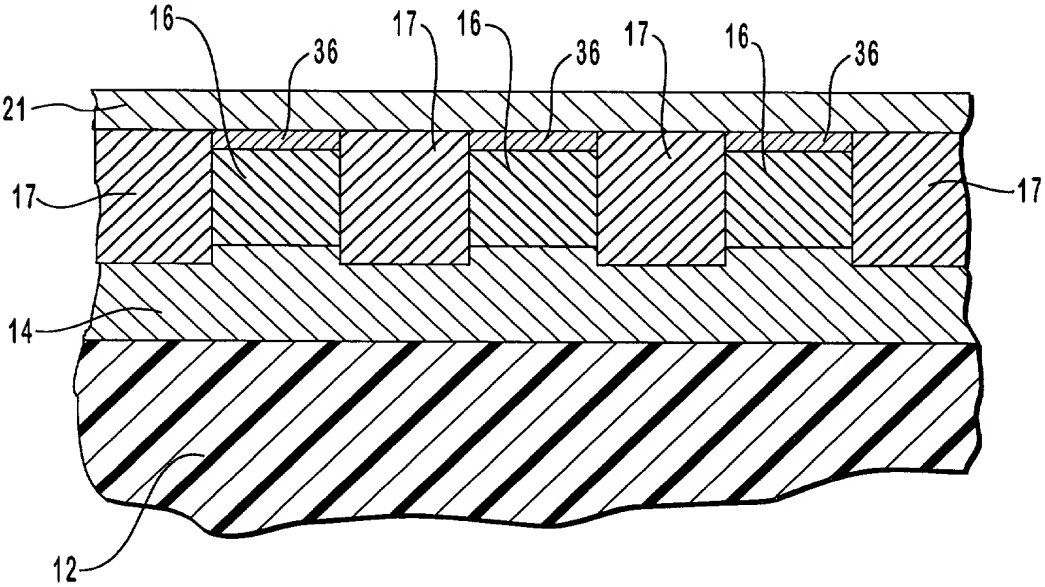


FIG. 4

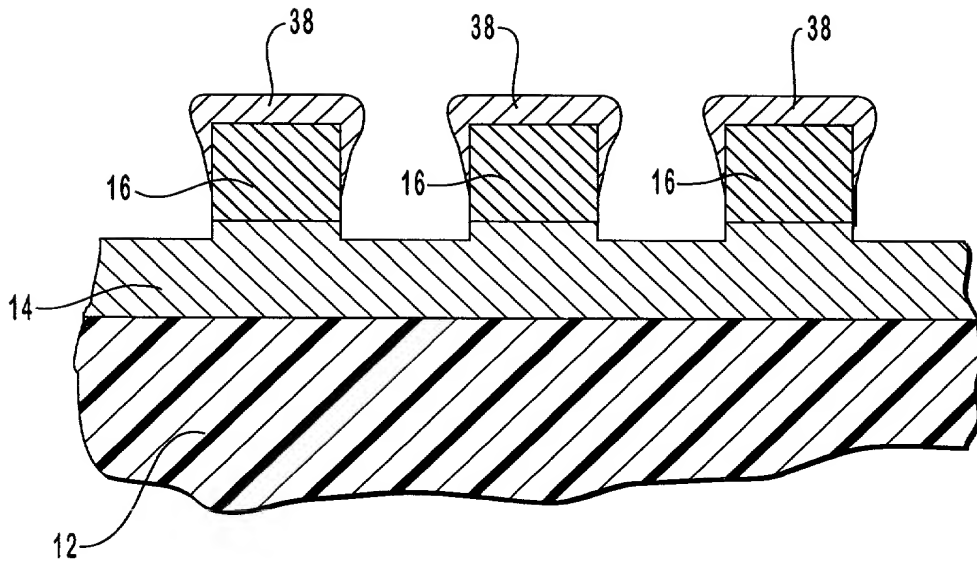


FIG. 5

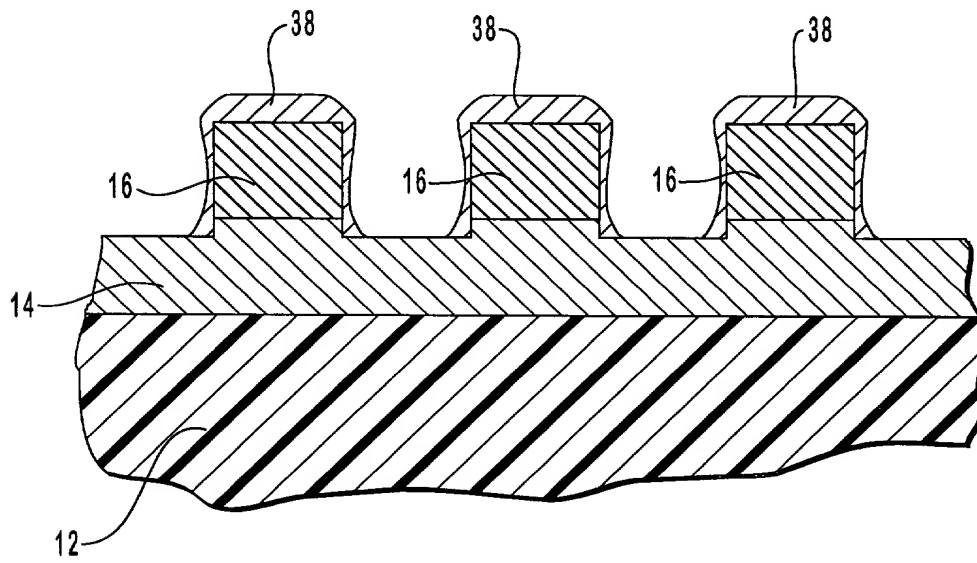
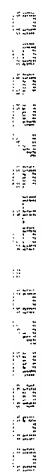
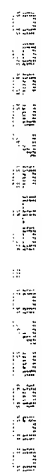
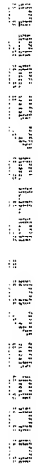


FIG. 6



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[illegible]



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DECLARATION, POWER OF ATTORNEY, AND PETITION

We, Gurtej Sandhu, a citizen of the United Kingdom, Anand Srinivasan, a citizen of India, and Ravi Iyer, a citizen of India, declare: that we are citizens as stated above; that our residences and post office addresses are 2964 East Parkriver Drive, Boise, Idaho, 83706, 670 South Clearwater, #201, Boise, Idaho, 83712, and 5600 South Fuchsia, Boise, Idaho, 83705, respectively; that we verily believe we are the original, first, and joint inventors of the subject matter of the invention or discovery entitled INTERLEVEL DIELECTRIC STRUCTURE AND METHODS FOR FORMING THE SAME for which a patent is sought and which is described and claimed in the specification attached hereto; that we have reviewed and understand the contents of the above-identified specification, including the claims referred to, and that we acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

Wherefore, we pray that Letters Patent be granted to us for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, Idaho, this 5th day of July, 1996.

Inventor:

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Signed at BOISE, Idaho, this 5th day of JULY, 1996.

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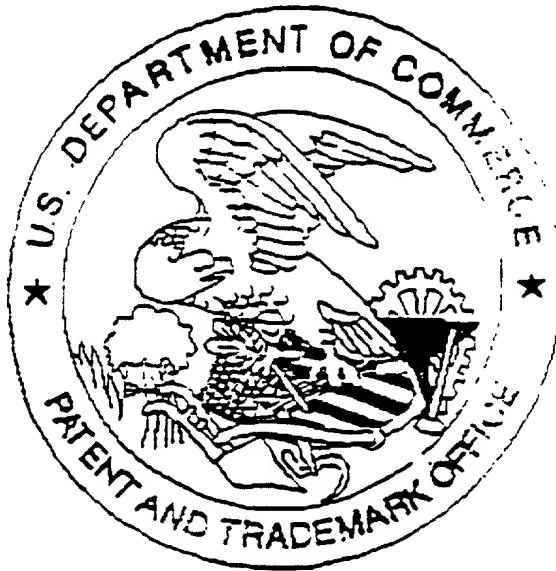
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☐ Page(s) _____ of _____ were not present
for scanning. (Document title)

☐ Page(s) _____ of _____ were not present
for scanning. (Document title)

There are 21 pages of Specification enclosed

☐ Scanned copy is best available.

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